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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,028	09/29/2003	Sameer P. Pendharker	TI-33654	9934

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EXAMINER	
DOAN, THERESA T	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,028	PENDHARKER ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-12* is/are rejected.

7)☒ Claim(s) *13-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/08/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 2-15 and cancelled claims 1 and 16 in the reply filed on 08/15/05 is acknowledged.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) **"d"** mentioned in the description of the specification on page 6, paragraph [0032], line 5. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

3. The prior art documents submitted by applicant in the Information Disclosure Statement filed on 12/08/03, have all been considered and made of record (note the attached copy of form PTO-1449).

Claim Objections

4. Claims 2 and 13 are objected to because of the following informalities:

- In claim 2, line 1, " : " should be inserted right after a word "**comprising**".

- In claim 13, line 1, a phrase "**the** drain plug" should be changed to "**a** drain plug".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 2-3 and 5-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishizawa (U.S. Pat. 4,404,575).

Regarding claim 2, Nishizawa (Fig. 1) discloses an integrated-circuit device, comprising:

a substrate 11 (column 2, line 66), having a top surface and a bottom surface;

a first region near the top surface (corresponding to the top portion of layer 12, see Fig. 1 labeled by the examiner below);

a first and second gate regions 14 in the first region (column 3, line 2), each having a top surface, a bottom surface and a side surface;

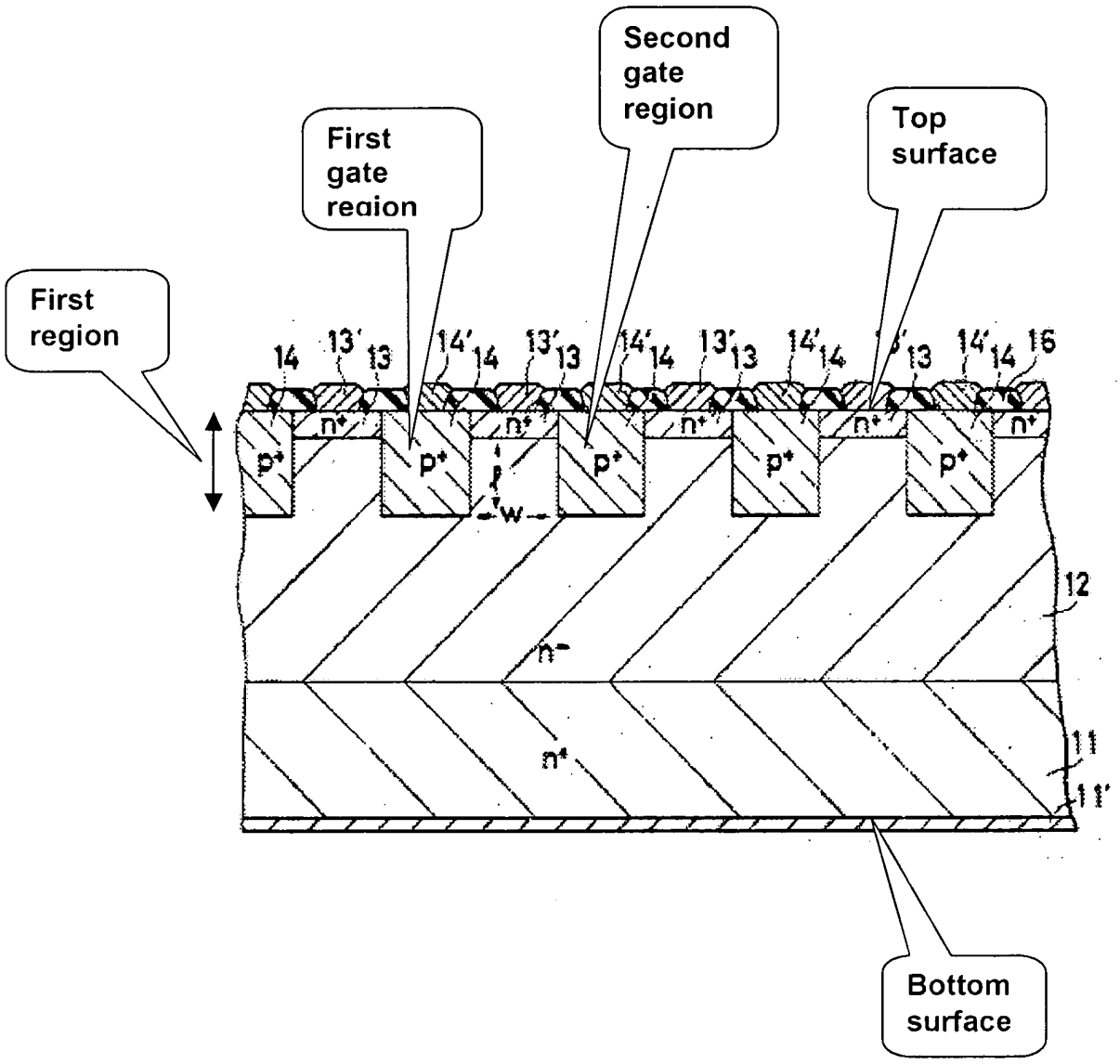
the side surfaces of the first and second gate regions 14 being substantially parallel to each other and substantially perpendicular to the top surface of the substrate 11 (see Fig. 1 Labeled by the examiner below);

the top surface of the first gate region 14 being electrically communicable to a gate terminal 14' (column 3, lines 2-5);

a channel region (W) in the first region, between the first and the second gate regions 14 (column 3, lines 10-15) having side surfaces adjacent to the side surfaces of the gate regions 14, a top surface, and a bottom surface; and

the top surface of the channel region (W) electrically communicable to a source terminal 13', the bottom surface of the channel region (W) electrically communicable to a drain terminal 11'.

FIG. 1


First region
First gate region
Second gate region
Top surface
Bottom surface
14
13'
13
14'
16
n+
p+
W
12
n-
11
11'

Regarding claim 3, Nishizawa (Fig. 1) discloses that the channel region (W) passes an electric current from the source region 13 to the drain region 11 in a direction substantially perpendicular to the top surface of the substrate 11 upon a biasing voltage being applied between the source terminal 13' and the drain terminal 11' (column 5, lines 64-68 through column 6, lines 1-7), and the magnitude of the current in the channel region is controllable with a biasing voltage at the gate terminal 14' (column 3, lines 48-56).

Regarding claims 5-6, Nishizawa further discloses an n-type buried layer 12. It is noted that the process limitation (doped with antimony) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 7-8, Nishizawa discloses that the first region of layer 12 is formed by an n-type epitaxial growth technique (column 2, lines 67-68).

Regarding claim 9, Nishizawa (Fig. 1) discloses that the substrate 11 is a bonded wafer having a bonded layer 12 formed thereon.

Regarding claim 10, Nishizawa discloses that the first gate region (14 or 24 in Fig. 6) has a pill-box shape with a substantially flat top surface and bottom surface and a side surface substantially perpendicular to the top and bottom surfaces.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa (U.S. Pat. 4,338,618) in view of Nishizawa (U.S. Pat. 4,404,575).

Regarding claim 2, Nishizawa'618 (Fig. 7) discloses an integrated-circuit device, comprising:

a substrate 113 (column 6, lines 20-22), having a top surface and a bottom surface;

a first region 114 near the top surface;

a first and second gate regions (122,123) in the first region 114 (column 7, lines 9-10), each having a top surface, a bottom surface and a side surface;

the side surfaces of the first and second gate regions (122,123) being substantially parallel to each other and substantially perpendicular to the top surface of the substrate 113 (see Fig. 7 Labeled by the examiner below);

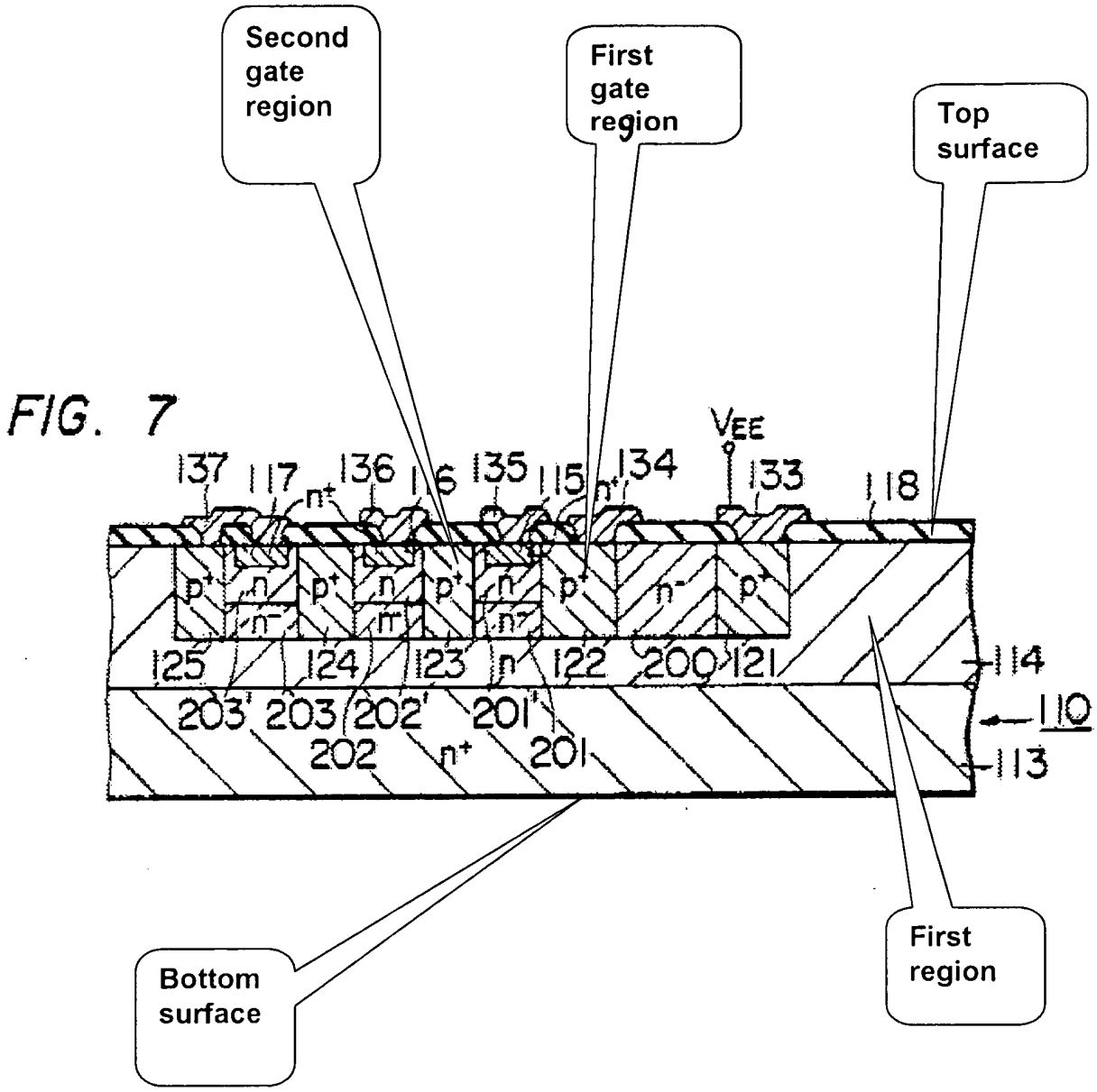
the top surface of the first gate region 122 being electrically communicable to a gate terminal 134;

a channel region 201 in the first region 114 (column 9, lines 22-26), between the first and the second gate regions (122,123) having side surfaces adjacent to the side surfaces of the gate regions (122,123), a top surface, and a bottom surface (column 9, lines 32-34); and the top surface of the channel region 201 electrically communicable to a drain terminal 135 of a drain region 115 (column 7, line 10), the bottom surface of the channel region 201 electrically communicable to a source terminal 113 (column 7, lines 13-15).

Nishizawa'618 does not disclose that the drain region 115 can serve as a source region, and the source region 113 can serve as a drain region.

However, Nishizawa'575 (Fig. 8) teaches a semiconductor device having the top surface of the channel region 22 electrically communicable to a source region 23, the bottom surface of the channel region 22 electrically communicable to a drain region 21. In addition, the drain region 21 can serve as the source region and the source region 23 can serve as the drain region in order to form an inverse operation (column 7, lines 12-17). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device structure of Nishizawa'618 by forming the source region 113 serves as a drain region and the drain region 115 serves as a source region in order to form an inverse operation, as taught by Nishizawa'575 (column 7, lines 12-17).

FIG. 7


Second gate region
First gate region
Top surface
Bottom surface
First region
V_{EE}
137
117
136
116
135
115
134
133
118
n^+
p^+
n^-
125
124
123
122
200
121
114
110
113
203'
203
202'
201'
202
201

Regarding claim 3, Nishizawa'618 (Fig. 7) discloses that the channel region 201 passes an electric current from the drain region 115 to the source region 113 in a direction substantially perpendicular to the top surface of the substrate upon a biasing voltage being applied between the source terminal 113 and the drain terminal 115 (column 11, lines 4-8), and the magnitude of the current in the channel region is controllable with a biasing voltage at the gate terminal 122 (column 7, lines 42-49).

Regarding claim 4, Nishizawa'618 discloses that the substrate formed under the layer 113 is a p-type silicon (not shown, see column 6, lines 25-28).

Regarding claims 5-6, Nishizawa'618 further discloses that the layer 113 is alternatively formed to be an n-type buried layer in the p-type substrate (column 6, lines 25-27). It is noted that the process limitation (doped with antimony) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 7-8, Nishizawa'618 discloses that the first region 114 is formed by an n-type epitaxial growth technique (column 6, lines 20-25).

Regarding claim 9, Nishizawa'618 discloses that the substrate is a bonded wafer 110 (column 6, lines 20-22).

Regarding claim 10, Nishizawa'618 discloses that the first gate region 122 has a pill-box shape with a substantially flat top surface and bottom surface and a side surface substantially perpendicular to the top and bottom surfaces (see Fig. 7 above).

Regarding claim 11, Nishizawa'618 discloses that the channel region 201/202 has a ring shape enclosing the first gate region 123, a bottom surface substantially coplanar to the bottom surface of the first gate region 123 and a top surface substantially coplanar to the top surface of the first gate region 123.

Regarding claim 12, Nishizawa'618 discloses that the second gate region 124/123 has a ring shape enclosing the channel region 202, a bottom surface substantially coplanar to the bottom surface of the first gate region 123 and a top surface substantially coplanar to the top surface of the first gate region 123.

Allowable Subject Matter

9. Claims 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose all the limitations recited in the above claims. Specifically, the prior art of record fails to disclose the drain plug region has a ring shape enclosing the second gate region, a bottom surface substantially coplanar to

the bottom surface of the first gate region and a top surface substantially coplanar to the top surface of the first gate region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T Doan

Theresa Doan
October 25, 2005.